PROJECT STATUS REPORT

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| Course : | B.Tech (Electronics and Communication Engineering) |
| Project name : | Implementation Of Vision For Robots On FPGA |

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| Completed WORK | | | |
| **DATE** | **STATUS** | **DETAILS** | |
| 11/01/2021 | Completed | Implementation of vision for robots on FPGA topic is selected. | |
| 18/01/2021 | Completed | Literature survey on IJCV paper Distinctive Image Features from Scale-Invariant Keypoints | |
| 09/02/2021 | Completed | Installation of Xilinx Software | |
| 21/02/2021 | Completed | Implementation of basic circuits in VHDL using Xilinx | |
| 18/04/2021 | Completed | Literature survey on different research papers | |
| 22/05/2021 | Completed | Abstract verification | |
| 30/05/2021 | Completed | Implemented SIFT in python using Open CV library | |
| 14/06/2021 | Completed | Implemented SIFT in Matlab and Simulink | |
| 28/06/2021 | Completed | Implemented SIFT Feature Descriptor Sysgen Model in Xilinx System Generator | |

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| **DATE** | **STATUS** | **DETAILS** |
|  | Yet to be done | Conversion of Sysgen Model to HDL code |
|  | Yet to be done | Verification of the implementation for real time data |
|  | Yet to be done | Documentation work |

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| **PROJECT STATUS** | | | | |
| **OVERALL  PROJECT  STATUS** | **50% COMPLETED** | **SUMMARY** | Implemented SIFT Feature Descriptor Sysgen Model in Xilinx System Generator to generate HDL Code | |
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**Project Students Project Guide**

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